V_{our} In the illustrated embodiment of FIG. **12**, the circuit **630** is a reset integrator operating as a form of transimpedence amplifier. The circuit **630** includes a differential amplifier **632** with the offset corrected current I_{out} provided to a first input thereof and a reference voltage V_{ref} coupled to the second input thereof. The feedback in turn is provided by a feedback capacitor **634**. A reset switch **636** is also provided to reset the amplifier **632**, in particular where circuit **630** is shared between a plurality of detector elements in a time multiplexed manner.

It will be appreciated by those skilled in the art that additional embodiments of a current to voltage conversion circuit **630** may be implemented including a more conventional transimpedence circuit employing a feedback resistor. The embodiment illustrated in FIG. **12** is preferred, however, for VLSI implementations due to the difficulty in implementing large resister values accurately and uniformly in VLSI circuits.

While the foregoing detailed description of the invention has been provided in terms of specific embodiments and specific circuit implementations, it will be appreciated by those skilled in the art that such are merely illustrative in nature and a variety of modifications may be made while remaining within the scope of the present invention. Accordingly, the present invention should not be limited to the aforedescribed preferred embodiments.

What is claimed is:

1. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals Provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises:

a correction circuit including a plurality of [parallel connected] circuit elements; and

means for selectively electrically connecting said circuit elements into the detector readout circuit in response to stored offset correction values; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

2. An infrared imaging system as set out in claim **1**, wherein said plurality of [parallel connected] circuit elements comprise a plurality of capacitors.

3. An infrared imaging system as set out in claim **2**, wherein said capacitors have capacitances of $2^N C_0$, respectively, where C_0 is a fixed capacitance and N is a nonnegative integer.

4. An infrared imaging system as set out in claim **3**, wherein there are four capacitors having respective capacitances of C_0, $2C_0$, $4C_0$ and $8C_0$.

5. An infrared imaging system as set out in claim **1**, wherein said means for selectively connecting comprises a plurality of switches, equal in number to said plurality of [parallel connected] circuit elements and connected in series therewith.

6. An infrared imaging system as set out in claim 1, wherein said offset correction values are binary values and wherein said means for storing comprises a digital memory.

7. An infrared imaging system as set out in claim 6, wherein said digital memory stores a separate binary offset correction value for each detector element in the array.

8. An infrared imaging system as set out in claim 1, wherein said plurality of detector elements are arranged in a plurality of rows and columns and wherein said means for correcting comprises a separate offset correction circuit for each column and wherein said means for providing said offset correction values provides said offset correction values in a time multiplexed manner to said means for correcting.

9. An infrared imaging system as set out in claim 1, wherein said plurality of parallel connected circuit elements comprise a plurality of constant current sources.

10. An infrared imaging system as set out in claim 9, wherein said current sources provide substantially constant currents of $2^N I_o$, respectively, when coupled into said readout circuit by said means for selectively connecting, where I_o is a fixed current value and N is a nonnegative integer.

11. An infrared imaging system as set out in claim 10, wherein there are four constant current sources providing substantially constant currents of I_o, $2I_o$, $4I_o$ and $8I_o$.

12. An infrared imaging system as set out in claim 1, wherein said array of detector elements and said readout circuit are formed as a single monolithic integrated circuit chip.

13. An infrared imaging system as set out in claim 1, wherein said plurality of detector elements comprise microbolometer detector elements.

14. An infrared imaging system as set out in claim 13, wherein said means for biasing comprises a constant current source coupled to said microbolometer detector elements.

15. An infrared imaging system as set out in claim 13, wherein said means for biasing comprises a fixed voltage source coupled to said microbolometer detector elements.

16. An infrared imaging system as set out in claim 15, wherein said means for correcting comprises a plurality of substantially constant current sources selectively coupled to said voltage source and in parallel with said microbolometer detector elements.

17. An infrared imaging system as set out in claim 16, wherein said means for correcting further comprises a plurality of switches coupled in series with respective constant current sources.

18. An infrared imaging system as set out in claim 17, wherein said offset correction values comprise an on or off signal supplied to each of said switches.

19. An infrared imaging system as set out in claim 1, wherein said output means comprises one or more output buffers.

20. An infrared imaging system as set out in claim 1, wherein said focal plane array further comprises a differential amplifier with first and second inputs wherein the first input is electrically connected to the readout circuit so as to receive the detection signals and wherein the second input is connected to an adjustable reference voltage.

21. An infrared imaging system as set out in claim 1, further comprising timing means for providing focal plane timing signals to said readout circuit.

22. An infrared imaging system as set out in claim 21, wherein said readout circuit further comprises offset correction logic means for controlling the means for correcting in response to said timing signals provided from the timing means.

23. An infrared imaging system as set out in claim 22, wherein said offset correction logic means receives said offset correction values from said means for storing and provide them to said means for correcting in response to said timing signals.

24. An infrared imaging system as set out in claim 1, further comprising means, coupled to said output means, for analog to digital converting the corrected detection signals and providing corresponding image data for each detector element.

25. An infrared imaging system as set out in claim 24, further comprising a memory for temporarily storing image data corresponding to all the detector elements of the array.

26. An infrared imaging system, comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising a plurality of readout cells equal in number to the plurality of detector elements, means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements, wherein said means for correcting comprises an offset correction circuit in each readout cell of the readout circuit and wherein each offset correction circuit comprises a plurality of [parallel connected] circuit elements and means for selectively electrically connecting said circuit elements into the readout cell in response to a stored offset correction value corresponding to said readout cell; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

27. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the analog detection signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting

comprises a plurality of [capacitors] circuit elements connected between said sample node and a reference voltage and a corresponding plurality of switches coupled in series with each respective [capacitor] circuit elements and said reference voltage, wherein said plurality of switches are selectively turned on or off to provide a desired amount of discrete offset correction for each detector element.

28. An infrared focal plane array as set out in claim 27, wherein said readout circuit further comprises means for controlling said means for correcting so as to selectively open and close said plurality of switches in a time multiplexed manner during readout of a plurality of separate detector elements.

29. An infrared focal plane array as set out in claim 27, wherein said detector elements comprise microbolometer detector elements.

30. An infrared focal plane array as set out in claim 29, wherein said means for said biasing comprises a constant current source coupled to said microbolometer detector elements and said sample and hold capacitor.

31. An infrared focal plane array as set out in claim 27, wherein said readout circuit further comprises a differential amplifier having first and second inputs, the first input thereof coupled to said sample node and said second input thereof coupled to a adjustable voltage source.

32. An infrared focal plane array as set out in claim 31, wherein said readout circuit further comprises a feedback capacitor coupled between the output of the differential amplifier and said first input thereof.

33. An infrared focal plane array as set out in claim 32, wherein said readout circuit further comprises a switch coupled between and parallel with said feedback capacitor between the output of the differential amplifier and the first input thereof.

34. An infrared focal plane array as set out in claim 27 wherein said plurality of detector elements and said readout circuit are formed as a single monolithic integrated circuit wherein said readout circuit acts as a substrate for said detector elements.

35. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

a sample and hold capacitor;

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon, wherein the analog detection signal is a voltage signal provided at a sample node coupled to the sample and hold capacitor; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, wherein the discrete offset correction varies from detector element to detector element and comprises an offset correction voltage added to, or subtracted from, the voltage signal, wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node, and wherein said means for correcting comprises a plurality of [parallel connected] constant current sources connected between said sample node and a reference voltage and a plurality of switches corresponding to said plurality of constant current sources and respectively coupled in series therewith.

36. An infrared imaging system as set out in claim 1, wherein said plurality of circuit elements are parallel connected.

37. An infrared imaging system as set out in claim 26, wherein said plurality of circuit elements are parallel connected.

38. An infrared imaging system as set out in claim 27, wherein said plurality of circuit elements comprise capacitors.

39. An infrared imaging system as set out in claim 35, wherein said plurality of circuit elements are parallel connected.

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